

Amendments to the Claims

1. (Currently Amended) An IC-circuit construction, comprising:

a ~~where~~ the circuit ~~[[is]]~~ partitioned into multiple power consuming sub-circuits, the sub-circuits including a first and a second power supply terminal ~~which each has to receive ~~[[a]]~~~~
supply voltage, and ~~where~~ the sub-circuits ~~[[are]]~~ connected in series, a first sub-circuit receiving
a first input voltage level at its first power supply terminal, and a second voltage level output at
the second power supply terminal of the first sub-circuit being used as input voltage level in a
second sub-circuit; and ~~where~~

a control-circuit is ~~provided in order~~ configured to balance ~~[[the]]~~ voltage drops across
the power consuming sub-circuits to maintain ~~whereby~~ constant voltage-drops over the power
consuming sub-circuits, the control-circuit including

~~are maintained, and ~~where~~ ground voltage level (VHH) in the power supply a first sub-~~
circuit is used as the supply voltage level in a second sub-circuit and ~~where the control circuit~~
comprises

a first buffer capacitor coupled in parallel over the supply voltage level (VBB)
first power supply terminal and ground voltage level (VHH) the second power supply terminal of
the first sub-circuit, ~~[[and]]~~

a second buffer capacitor coupled in parallel over the supply voltage level (VHH)
first power supply terminal and the ground voltage level (GND) second power supply terminal of
the second sub-circuit, ~~whereby means for maintaining a uniform voltage drop over the first and~~
the second buffer capacitor comprises and

at least one bucket capacitor ~~which is~~ alternately coupled in parallel over the first and the second buffer capacitor through a switching system controlled by a toggling signal.

2. (Currently Amended) The IC-circuit construction ~~IC-circuit~~ as claimed in claim 1, wherein the control circuit includes:

~~there are~~ two bucket capacitors that get switched at the same time ~~such as~~ to alternately couple to the first and the second buffer capacitor respectively.

3. (Currently Amended) The IC-circuit construction ~~IC-circuit~~ as claimed in claim 1 or 2, wherein the switching system ~~switches for alternately coupling the bucket capacitors are~~ is controlled by one of a free-running oscillator[[,]] and a clock, ~~or some other suitable signal of~~ periodic or nonperiodic nature.

4. (Currently Amended) The IC-circuit construction as claimed in claim 1, wherein the power consuming sub-circuits are digital or analog or mixed signal circuits.

5. (Currently Amended) The IC-circuit construction ~~IC-circuit~~ as claimed in claim 1, ~~whereby~~ wherein each of the power consuming sub-circuits ~~[[are]]~~ is located on ~~each their~~ its respective chip.

6. (Currently Amended) The IC-circuit construction ~~IC-circuit~~ as claimed in claim 1, ~~whereby~~ wherein the ~~control circuit~~ control-circuit is designed ~~such as~~

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configured to maintain different voltage drops across the multiple power
consuming sub-circuits.